

1 What is claimed is:

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3 1. A method of forming an integrated circuit comprising the steps of:
4 forming circuit function block on an IC chip; and
5 forming a decoupling capacitor in an area above the circuit function block.

6

7 2. The method of claim 1, wherein the step of forming an integrated circuit further
8 comprising the step of:

9 forming a top metal layer;

10 forming a bottom metal layer; and

11 forming an inter-digitated capacitance structure between the top metal layer and
12 bottom metal layer, wherein the inter-digitated capacitance structure is operated on to
13 generate a predetermined pattern of inter-digitated metal fingers.

14

15 3. The method of claim 2, wherein the step of forming an inter-digitated capacitance
16 structure comprising the steps of:

17 forming an at least one inter-digitated metal;

18 forming a plurality of inter-digitated metal fingers extending outward from the at
19 least one inter-digitated metal; and

20 forming dielectric material, which is deposited between the at least one inter-
21 digitated metal fingers.

22

23 4. The method of claim 3, wherein the step of forming a dielectric material further
24 comprises the step of:

25 forming a first dielectric layer below the inter-digitated metal fingers and the
26 bottom metal layer, wherein the first dielectric layer has a predetermined thickness.

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- 1 **5.** The method of claim 4, wherein the first dielectric layer is a low dielectric
2 material.
3
- 4 **6.** The method of claim 3, wherein the step of forming an inter-digitated capacitance
5 structure further comprising the step of:
6 forming a second dielectric layer between the inter-digitated metal fingers and the
7 top metal layer.
8
- 9 **7.** The method of claim 6, wherein the second dielectric layer comprises a
10 predetermined dielectric material.
11
- 12 **8.** The method of claim 3, wherein the first metal layer is a plate which isolates the
13 de-coupling capacitor from the circuit block.
14
- 15 **9.** The method of claim 2, wherein the step of forming an inter-digitated capacitance
16 structure further comprising the steps of:
17 forming a inter-layer dielectric layer below the bottom metal layer.
18
- 19 **10.** The method of claim 3, wherein the step of forming an inter-digitated capacitance
20 structure comprises the step of:
21 forming a plurality of de-coupling capacitances between the inter-digitated
22 capacitance structure, the top metal layer and bottom metal layer, and the first dielectric
23 layer and second dielectric layer.
24
- 25 **11.** A method of forming an integrated circuit comprising the steps of:
26 forming a circuit function block on an IC chip;
27 forming a first metal layer separating a decoupling capacitor circuit from the
28 circuit function block; and

1 forming an inter-digitated capacitance structure on the first metal layer, wherein
2 the inter-digitated capacitance structure is etched to form a predetermined pattern of inter-
3 digitated metal fingers.

4
5 **12.** The method of claim 11, wherein the inter-digitated capacitance structure
6 comprises the steps of:
7 forming at least one inter-digitated metal finger; and
8 forming a dielectric layer is deposited between the at least one inter-digitated metal
9 finger.

10
11 **13.** The method of claim 11, the step of forming an integrated circuit further
12 comprising the step of:
13 forming a first dielectric layer above the circuit function block and the inter-
14 digitated capacitance structure, such that the first dielectric layer has a predetermined
15 thickness.

16
17 **14.** The method of claim 13, wherein the first dielectric material is a low dielectric
18 material.

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20 **15.** The method of claim 11, further comprising the steps of:
21 forming a second dielectric layer above the bottom metal plate.

22
23 **16.** An integrated circuit comprising:
24 a circuit function block having a predetermined circuit layout; and
25 an inter-digitated capacitance structure comprising at least one metal plate and a
26 plurality of inter-digitated metal fingers on top of the circuit function block.

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1 **17.** The integrated circuit of claim 16, wherein a plurality of de-coupling capacitances
2 are formed between the inter-digitated capacitance structure and first and second metal
3 layers.

4
5 **18.** The integrated circuit of claim 16, further comprising:
6 a first dielectric layer formed on the circuit function block;
7 a third dielectric layer formed on the second metal layer; and
8 a third metal plate formed on the third dielectric layer.

9
10 **19.** The integrated circuit of claim 16, further comprising:
11 a second dielectric layer formed on top of the first metal layer.

12
13 **20.** The integrated circuit of claim 16, wherein the inter-digitated metal fingers extend
14 from the metal plate in such a manner that the plurality of inter-digitated metal fingers are
15 in parallel and have a predetermined separation and width.